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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,076	10/04/2005	Andrei Terechko	NL 030344	8796

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EXAMINER	
VICARY, KEITH E	
ART UNIT	PAPER NUMBER
2183	
MAIL DATE	DELIVERY MODE
10/12/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,076	TERECHKO, ANDREI	
	Examiner	Art Unit	
	KEITH VICARY	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/2/2010 has been entered.

Specification

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

a. In page 1, line 6, “operation” should be “operations”.

b. In page 1, line 16, “restrains rather than computation restrains” should be “restraints rather than computation restraints”.

c. In page 1, line 22, “In a clustered processor resources, like” should be “In a clustered processor, resources like”.

d. In page 3, line 33, “register” should be “registers”.

e. In page 5, line 17, “op4” should be “op5”.

Claim Objections

3. Claims 1 and 5 are objected to because of the following informalities. Appropriate correction is required.

f. In claim 1, line 10, “dedicated direct signal data signal connection” should be “dedicated direct data signal connection” to eliminate the redundancy of using "signal" twice. Also, see page 4, lines 18-29, which uses the term “dedicated direct data signal connection”.

g. In claim 5, line 10, “dedicated direct signal data signal connection” should be “dedicated direct data signal connection” to eliminate the redundancy of using "signal" twice. Also, see page 4, lines 18-29, which uses the term “dedicated direct data signal connection”.

h. In claim 5, line 8, “clusters” should be “said clusters" akin to claim 1, so that it is not indefinite as to whether "said clusters” of the last line refers to “a plurality of clusters” of line 2 or a potentially different “clusters” of line 8.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 1 recites the limitation “one or more pipeline registers arranged in both said control connections, depending on the distance between said instruction unit and said clusters, and in a dedicated direct signal data signal connection between any two of said clusters” in lines 7-10.

It is indefinite as to how, or if, the one or more pipeline registers that are arranged in "said control connections” are the same as the one or more pipeline registers that are arranged “in a dedicated direct signal data signal connection between any two of said clusters”.

In the instant disclosure (particularly page 4, lines 18-29 which have been cited by applicant), the pipeline register that is arranged in the control connection paths, in order to pipeline the control signals, is not described as being between any two of the clusters.

Consequently, one skilled in the art cannot reasonably ascertain how, or if, the pipeline registers that are arranged in "said control connections” are the same as the pipeline registers that are arranged “in a dedicated direct signal data signal connection between any two of said clusters”, and the claims thus fail to pass muster under 35 U.S.C. 112, second paragraph.

i. Claims 2-4 are rejected for failing to alleviate the rejection of claim 1 above.

7. Claim 5 recites the limitation “one or more pipeline registers arranged in both said control connections, depending on the distance between said instruction unit and

clusters, and in a dedicated direct signal data signal connection between any two of said clusters" in lines 7-10.

It is indefinite as to how, or if, the one or more pipeline registers that are arranged in "said control connections" are the same as the one or more pipeline registers that are arranged "in a dedicated direct signal data signal connection between any two of said clusters".

In the instant disclosure (particularly page 4, lines 18-29 which have been cited by applicant), the pipeline register that is arranged in the control connection paths, in order to pipeline the control signals, is not described as being between any two of the clusters.

Consequently, one skilled in the art cannot reasonably ascertain how, or if, the pipeline registers that are arranged in "said control connections" are the same as the pipeline registers that are arranged "in a dedicated direct signal data signal connection between any two of said clusters", and the claims thus fail to pass muster under 35 U.S.C. 112, second paragraph.

j. Claims 6-8 are rejected for failing to alleviate the rejection of claim 5 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US 5598408).

10. Consider claim 1, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108) each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these are instruction paths), wherein said instruction unit is connected to each of said clusters via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108), and a dedicated direct signal data signal connection between any two of said clusters (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

However, Batten does not disclose of one or more pipeline registers arranged in both said control connections, depending on the distance between said instruction unit and said clusters, and between any two of said clusters.

On the other hand, Nickolls does disclose of one or more pipeline registers arranged depending on distance between elements (col. 6, lines 11-14, partitioning a

message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 20, lines 11-15 discloses of pipeline registers in the path connecting different processor elements; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

11. Consider claim 2, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

12. Consider claim 3, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

13. Consider claim 5, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108)

each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these are instruction paths), wherein said instruction unit is connected to each of said clusters via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108), and a dedicated direct signal data signal connection between any two of said clusters (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

However, Batten does not disclose of one or more pipeline registers arranged in both said control connections, depending on the distance between said instruction unit and clusters, and between any two of said clusters.

On the other hand, Nickolls does disclose of one or more pipeline registers arranged depending on distance between elements (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 20, lines 11-15 discloses of pipeline registers in the path connecting different processor elements; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

14. Consider claim 6, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

15. Consider claim 7, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

16. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claims 3 and 7 above, and further in view of Pechanek et al. (Pechanek) (US 5659785).

17. Consider claim 4, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

18. Consider claim 8, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten

and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

Response to Arguments

19. Applicant argues on pages 4-5 that the amended limitations are well within the requirements of 35 U.S.C. 112, second paragraph, and thus the rejection can no longer be sustained.

However, the amended limitations do not overcome the indefinite rejection, as explained in the 112 rejection section above.

Specifically, it is indefinite as to how, or if, the one or more pipeline registers that are arranged in "said control connections" are the same as the one or more pipeline registers that are arranged "in a dedicated direct signal data signal connection between any two of said clusters".

In the instant disclosure (particularly page 4, lines 18-29 which have been cited by applicant), the pipeline register that is arranged in the control connection paths, in order to pipeline the control signals, is not described as being between any two of the clusters.

Consequently, one skilled in the art cannot reasonably ascertain how, or if, the pipeline registers that are arranged in "said control connections" are the same as the pipeline registers that are arranged "in a dedicated direct signal data signal connection between any two of said clusters", and the claims thus fail to pass muster under 35 U.S.C. 112, second paragraph.

Examiner generally notes that the advisory action had conveyed the examiner's preliminary opinion that the pending indefinite rejection would not be overcome, as the amended claims appeared to convey that any given pipeline register is arranged in both said control connections and a dedicated direct signal data signal connection. Examiner further notes that the instant indefinite rejection remains analogous to the Board's position (as explained in the BPAI decision dated 9/25/2009).

20. Applicant further argues that claims 2-16 and 18-26 are also allowable by virtue of its dependence from an allowable base claim.

However, examiner first notes that only claims 1-8 are pending. Furthermore, examiner notes that the final rejection dated 7/7/2010 conveyed that the examiner believed that the previously given rejection of the claims over the prior art remained relevant to the instant claims (as the Board reversed, pro forma, the examiner's rejection of the claims over the prior art, only because the claims were indefinite).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

k. Inoue et al. (US 5729758) disclose of a SIMD processor operating with a plurality of parallel processing elements in synchronization using pipeline registers.

l. Nolan (US 20060155956) discloses of delay elements for delaying communications with processor elements in order to achieve a degree of synchronization between operation of said processor elements.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH VICARY whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Keith Vicary/

Examiner, Art Unit 2183